REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 4 and 7 are pending and rejected. In addition, Claims 12-13 are new and Claims 4 and 7 are amended hereinabove.

The Applicants respectfully traverse the Examiner's restriction requirement that precipitated this divisional and therefore these claim changes. The Applicants reassert their election with traverse because, as the Applicants stated previously, "no reason exists for concluding that each Species has attained recognition in the art as a separate status or field of search." The Applicants position is supported by page 2 of the Office Action, where the Examiner argues that "CMOS includes both PMOS and NMOS." The Applicants submit that their position is further supported by the fact that both divisionals were prosecuted by the same Examiner as the parent case, both divisionals are being prosecuted in the same art unit, and both divisionals have pending Office Actions that are virtually identical to the pending Office Action in the parent case (the majority of the pending parent Office Action appears unchanged in the pending Office Actions of the two divisionals). Therefore, the Applicants fail to understand the justification for being forced to pay three application fees to have all of the inventions in the full claim set of the initial patent application prosecuted by the USPTO.

Amended Claim 4 positively recites that the cap layer of the NMOS transistor is separated from the gate oxide by a layer of oxide coupled to the lightly doped drain and a layer of nitride coupled to the lightly doped drain. These advantageously claimed features are not taught or suggested by the patents granted to Wang et al. or En et al.; either alone or in combination.

Wang et al. teaches a MOS transistor having a cap layer separated from the gate oxide by a single oxide layer (column 6 lines 39-45); not a layer of oxide plus a layer of nitride as advantageously claimed. Similarly, En et al. teaches a FET transistor having a cap layer separated from the gate oxide by a single aluminum oxide layer (column 6 lines 16-19); not a layer of oxide plus a layer of nitride as advantageously claimed.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 4 and respectfully assert that Claim 4 is patentable over the patents granted to Wang et al. and En et al.; either alone or in combination. Furthermore, Claim 12 is allowable for depending on allowable independent Claim 4 and, in combination, including limitations not taught or described in the references of record.

Amended Claim 7 positively recites that the cap layer of the NMOS transistor is separated from the gate oxide by a layer of oxide coupled to the lightly doped drain and a layer of nitride coupled to the lightly doped drain. These advantageously claimed features are not taught or suggested by the patents granted to Wang et al. or En et al.; either alone or in combination.

Wang et al. teaches a MOS transistor having a cap layer separated from the gate oxide by a single oxide layer (column 6 lines 39-45); not a layer of oxide plus a layer of nitride as advantageously claimed. Similarly, En et al. teaches a FET transistor having a cap layer separated from the gate oxide by a single aluminum oxide layer (column 6 lines 16-19); not a layer of oxide plus a layer of nitride as advantageously claimed.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 7 and respectfully assert that Claim 7 is patentable over the patents granted to Wang et al. and En et al.; either alone or in combination. Furthermore, Claim 13 is allowable for depending on allowable independent Claim 7 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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